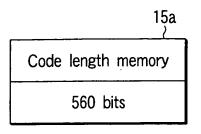


f Operation image of the output code	of the	output code generator	ıtor		
R-code	ے	01EDh	0013h		invalid
	ا م	00 00 00 01/11/10	111111111111111111111111111111111111111	(20021:12	
G-code	ا ح		invalid		7322h 0001h
	ا ا			11/00/11/10/	(0)(1)(0)(1)(0)(1)(0)(1)(0)(0)(0)(0)(0)(0)(0)(0)(0)(0)(0)(0)(0)
B-code	1		invalid		
R-enable	اح	FE00h	FFEOh		invalid
	ا م	11 11 11 10 00 00	0 00 00 00 00 11 11 11 11 11 16	10 00 00	
G-enable	ے		invalid		8000h FFF8h
	a P			10 00 00 00	10 00 00 00 00 00 00 00 11 11 11 11 11 1
/ B-enable	1		/ invalid	;	
					-
Buffer enable			Buffer 2		Buffer 6
Register 1	ا ا	01h	400		73h 00h
Register 2	اء	EDh	13h/		22h   01h
	ļ		<b>&gt;</b>		<b>&gt;</b>
Register 3	_ا م	3/11/11/11/11/10/11/3	11/10/11/1 0 0 1 1	1/	/////0//0/////////////////////////////
	<u>*</u>	R-cc	R-code data	<u> </u>	G-code data
Output code	ا ا	F6h	CFh		99h 11h



F I G. 3

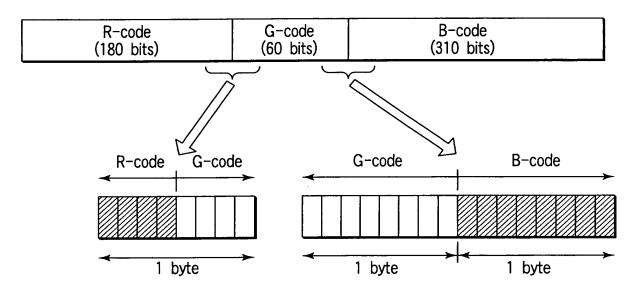
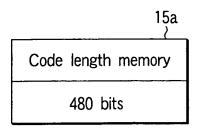


FIG.4



F I G. 5

	R-code (180 bits)	G-code (60 bits)	B-code (310 bits)
:	:	, :	:
N-6th	7 bits	8 bits	9 bits
N-5th	4 bits	5 bits	12 bits
N-4th	6 bits	10 bits	5 bits
N-3rd	13 bits	3 bits	8 bits
N-2nd	9 bits	8 bits	4 bits
N-1st	4 bits	6 bits	8 bits
Nth	10 bits	7 bits	3 bits

FIG. 6

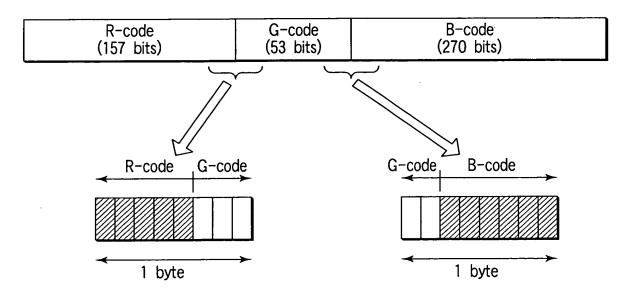


FIG. 7